In the Figures

Please amend Figure 12 as indicated in red on the attached sheet. A replacement sheet is additionally included.

REMARKS

Claims 1-23 were pending in the above-identified application and stand rejected. Applicants, having amended the claims, respectfully request reconsideration.

Amendments to the Figures

Applicants have amended Figure 12 to extend a lead to an appropriate signal line. This amendment addresses an obvious, minor drafting error, and does not add new matter.

Rejections Under 35 USC §102

Claims 1-23 stand rejected under §102(e) as being anticipated by Tamura et al. (6,707,727). Applicants address each rejection in turn.

Applicants' Invention

Applicants invention "relates to multi-level digital signaling, and in particular to techniques to equalize or compensate for errors that may otherwise be present in a multi-level, multi-line signaling system" (Spec., 1:6-9). "Such multi-level signaling is sometimes known as multiple pulse amplitude modulation or multi-PAM..." (Id. At 1:13-15). The invention is directed, at least in part, to "equalization mechanisms [that] may be particularly advantageous for multi-PAM communications systems" (Id. at 2:25-27). Multi-PAM signals differ from binary signals in that each signal level in a multi-PAM signal represents more than one distinct digital value. In the depiction of Applicants' Fig. 1, for example, a 4-PAM signal represents four two-bit "logical states" using four respective voltage levels VOUT0-VOUT3 (See e.g. page 5:9-31). The 4-PAM signal in the example of Fig. 1 thus represents four distinct digital values (00, 01, 11, and 10) using a voltage that varies between four distinct levels VOUT0-VOUT3.

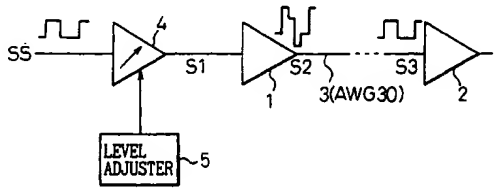
Tamura et al. (Tamura)

Tamura teaches drive circuits and techniques that equalize transmitted signals. Unlike the signals of Applicants' invention, however, Tamura does not appear to be directed to multi-PAM

signals. Instead, the Tamura drivers noted by the examiner adjust the output levels from a driver to compensate for waveform distortion or inter-code interference.

The examiner references col. 2, lines 26-65, of Tamura in rejecting applicants' claims. This portion does not appear to discuss multi-PAM signals. Tamura refers to this disclosure as relating to "a first aspect of the invention" (Tamura, 2:26). This first aspect is detailed elsewhere in connection with the figures. Tamura notes, for example, that "[t]he principle of the first aspect of the present invention will be explained with reference to FIG. 2" (Tamura, 9:64-65). Tamura's figure 2 is reproduced below in support of the following discussion.

Fig.2



Tamura's Figure 2

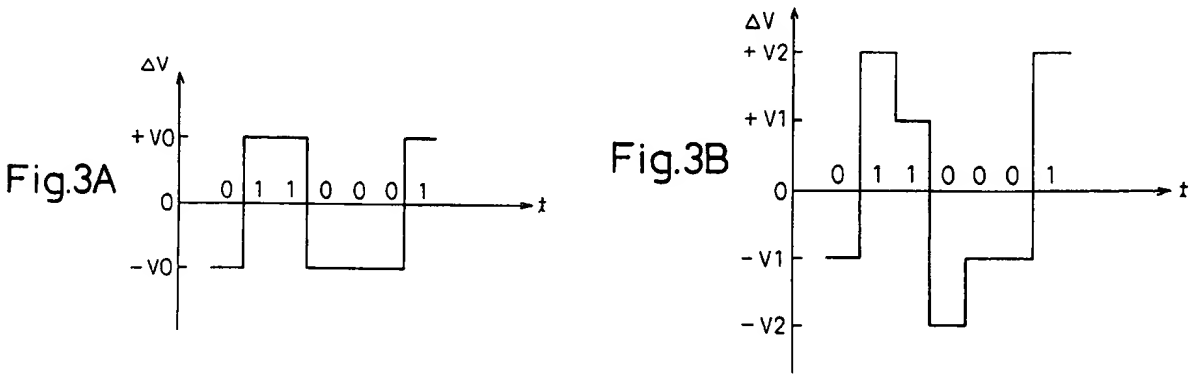
Tamura's Figure 2 depicts three waveforms corresponding to signals SS, S2, and S3. According to Tamura, a level adjuster 5 and front driver 4

> emphasize the high-frequency components of an input signal SS and generate a signal S1. The emphasized signal S1 is amplified by the output driver 1, and the amplified signal S2 is transmitted to the transmission line 3. The signal S2 is received by the receiver 2 as a signal S3. The signal S3 has a proper waveform with compensated high-frequency components and is free from distortion or inter-code interference.

(Tamura, 10:10-15) As seen in the foregoing Figure 2, and expressed in more detail in connection with Tamura's Figures 3A and 3B, the drive circuitry distorts the binary input signal SS to emphasize signal components that will be attenuated by the transmission line between the driver 1 and receiver 2. Ideally, the signal S3 "is free from distortion or inter-code interference" (*Ibid.*). In other words, the signal is distorted to counteract the effects of the channel. Tamura illustrates this concept in the example of Figure 2, *supra,* by illustrating the binary signal S3 as identical to the binary input signal SS.

Tamura describes the pre-emphasis provided to signal S2 by asserting that "the output of the

driver circuit ... provides one analog level (four analog levels are shown in FIG. 3B) instead of digital binary levels" (Tamura, 10:54-57). The signal S2 of Figure 2, a likeness of which is depicted in Figure 3B, is therefore representative of *binary* data, albeit distorted binary data. With reference to Tamura's Figures 3A and 3B, reproduced below, it is apparent that four signal levels +V2, +V1, -V1, and -V2 are used to represent just two distinct digital values: logic zero and logic one. Thus, though exhibiting more than two signal levels, the signal of Tamura's Fig. 3B is nevertheless binary. This intentionally distorted binary signal, in traversing the channel, suffers signal degradation that reforms the signal into a more typical binary pattern like that of Figure 3A.



Tamura's Figures 3A and 3B

All the signals SS, S1, S2, and S3 of Tamura are representative of just two distinct digital values, logic one and logic zero.

Claim Rejections

The examiner rejected all the claims as anticipated over Tamura under 35 USC §102. Applicants take each rejection in turn.

Claims 1-11

The examiner rejected claims 1, 12, and 20 over Tamura et al. Claim 1 recites "a driver circuit" that outputs "a signal having a voltage level that varies in time between at least three distinct levels *representative of at least three distinct digital values...*" (emphasis added). As noted above, the signals of Tamura represent but two distinct digital values, and thus do not meet the italicized language. Claim

1 further recites "a receiver circuit ... coupled to receive the signal [and] to determine which of the at least three distinct digital values is represented by the signal..." Turning to Tamura's Figure 2, reproduced above, the receiver 2 receives a binary signal S3 that represents a stream of ones and zeros. As such, Tamura's receiver 2 cannot "determine which of the at least three distinct digital values is represented by the signal" as claim 1 requires. Claim 1 therefore distinguishes the examples of Tamura's Figure 2. The remaining examples of Tamura likewise appear to teach binary signaling schemes, and consequently fail to anticipate claim 1 for at least the same reasons. The rejection of claim 1 as anticipated by Tamura should therefore be withdrawn.

Claims 2-11 depend from claim 1, and consequently distinguish Tamura for at least the same reasons claim 1 distinguishes. The rejections of claims 2-11 should therefore be withdrawn.

Claims 12-19

The examiner rejected claim 12 over Tamura et al. Claim 12, as amended herein, recites "a signaling device configured to produce a set of signal levels representing a set of at least three logical states..." The claimed signaling device includes "a main driver adapted to convert a plurality of binary input signals into an output signal that shifts over time between said signal levels to shift between said at least three logical states..." The expressed functionality is consistent with that of a multi-PAM driver, and precludes more typical binary drivers. Also consistent with multi-PAM, the claimed signaling device additionally includes "an equalization mechanism ... adapted to receive said plurality of binary input signals and generate a set of at least three equalization signals based on said binary input signals."

The signaling systems of Tamura do not convert binary input signals into output signals that shift between signal levels representing "at least three logical states" as does the system of claim 12. Furthermore, the equalizer mechanisms in Tamura do not appear to generate equalization signals "based upon [a] plurality of binary input signals" as does the equalization mechanism of claim 12. Tamura fails to anticipate claim 12 for at least these reasons. The rejection of claim 12 should therefore be withdrawn.

Claims 13-19

Claims 13-19 depend from claim 12, and consequently distinguish Tamura for at least the same reasons claim 12 distinguishes. The rejections of claims 13-19 should therefore be withdrawn.

Claim 20

The invention of claim 20 differs considerably from those of claims 1 and 12. In the system of claim 20, for example, there are two "main" drivers, "a first main driver adapted to receive a first plurality of input signals and to output ... a first signal [and] a second main driver adapted to receive a second plurality of input signals and to output ... a second signal..." There is additionally "an equalization mechanism." Of interest, the equalization mechanism is "configured to receive" the input signals to the first main driver and to compensate for crosstalk on the output from the second main driver. Support for claim 20 is found in e.g. applicants' figure 12 and the related text.

Applicants fail to see where the examiner has identified any circuitry in Tamura that develops equalization signals based upon the inputs to a first driver and applies those signals to the output of a second driver. As such, the examiner has failed to establish a *prima facie* case of anticipation with regard to claim 20. The rejection of claim 20 should therefore be withdrawn.

Claims 21-23

Claims 21-23 depend from claim 20, and consequently distinguish Tamura for at least the same reasons claim 20 distinguishes. The rejections of claims 21-23 should therefore be withdrawn.

CONCLUSION

In light of the foregoing remarks and amendments, the pending claims are in condition for allowance; accordingly, applicants respectfully request a Notice of Allowance. If the examiner's next action is other than the allowance of the pending claims, the examiner is requested to call applicants' attorney at (925) 621-2113.

Respectfully submitted,

Arthur J. Behiel
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on March 30, 2006

Laurie Moreno
Name

Signature

Mark-up Sheet

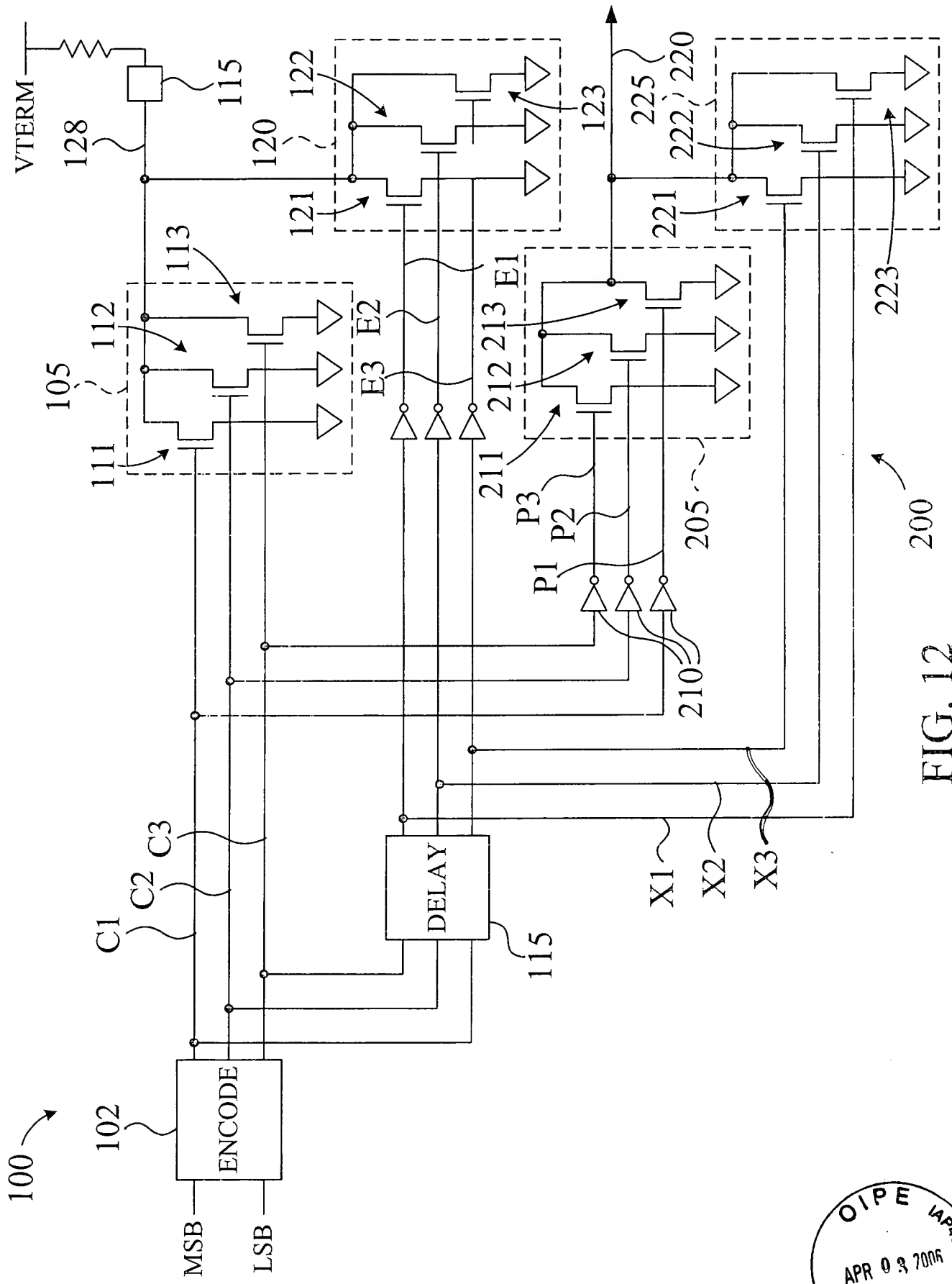

FIG. 12